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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/003,114	12/06/2001	Masaki Yamada	216932US2	5215

22850 7590 06/17/2005

OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C.
1940 DUKE STREET
ALEXANDRIA, VA 22314

EXAMINER	
MANDALA, VICTOR A	
ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 06/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H'A

Office Action Summary	Application No.	Applicant(s)	
	10/003,114	YAMADA ET AL.	
	Examiner	Art Unit	
	Victor A. Mandala Jr.	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3 and 5-31* is/are pending in the application.

4a) Of the above claim(s) *11-30* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5-10 and 31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Minhloan Tran
Primary Examiner
Art Unit 2826

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5/3/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3, 5-8, 10, and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent Application Publication No. 2003/0205815 Chung in view of U.S. Patent Application Publication No. 2004/0238965 Iwasaki et al.

1. Referring to claim 1, a semiconductor device comprising: a first interlayer insulating layer, (Chung Figure 4H organic low-k dielectric lower layer); a trench, (Iwasaki et al. Figure 9 #115 and Chung Figure 4H the are where it is labeled metal), formed in the first interlayer insulating layer, (Chung Figure 4H organic low-k dielectric lower layer); a barrier layer, (Iwasaki et al. Figure 9 #114b), formed in the trench, (Iwasaki et al. Figure 9 #115 and Chung Figure 4H the are where it is labeled metal); a conductive layer formed within the barrier layer, (Iwasaki et al. Figure 9 #114b), in the trench, (Iwasaki et al. Figure 9 #115 and Chung Figure 4H the are where it is labeled metal), the conductive layer, (Iwasaki et al. Figure 9 #115 and Chung Figure 4H the are where it is labeled metal), having a surface thereof higher than a highest surface of the first interlayer insulating layer, (Chung Figure 4H organic low-k dielectric lower layer), surrounding and adjoining the trench, (Iwasaki et al. Figure 9 #115 and Chung Figure 4H the are where it is labeled metal); an insulating film, (Chung Figure 4H inorganic low-k dielectric middle layer), having a flat surface and covering the first interlayer insulating layer,

(Chung Figure 4H organic low-k dielectric lower layer), and the conductive layer, (Iwasaki et al. Figure 9 #115 and Chung Figure 4H the are where it is labeled metal), the insulating film, (Chung Figure 4H inorganic low-k dielectric middle layer), configured to prevent diffusion of a conductor material, (Iwasaki et al. Figure 9 #115 and Chung claim 10 and Paragraph 0092 Line 17), in the conductive layer, (Iwasaki et al. Figure 9 #115 and Chung Figure 4H the are where it is labeled metal); and a second interlayer insulating layer, (Chung Figure 4H inorganic low-k dielectric upper layer), formed on the insulating film, (Chung Figure 4H organic low-k dielectric middle layer), the second interlayer insulating layer, (Chung Figure 4H inorganic low-k dielectric upper layer), having a high etching selective ratio, (Chung Paragraph 0090 Lines 28-30 & 34-35 and Paragraph 0106 Lines 16-20), to the insulating film, (Chung Figure 4H organic low-k dielectric middle layer).

** Chung teaches all of the claimed matter in claim 1, but is silent on a barrier layer formed in the trench where a conductive layer is formed within the barrier layer in the trench, but Iwasaki et al. does. It would have been obvious to one having skill in the art at the time the invention was made to form a barrier layer formed in the trench where a conductive layer is formed within the barrier layer in the trench because the barrier layer prevents the conductive layer from diffusing. The prevention of the conductive layer from diffusing prevents the creation of voids and inter-connect breakdowns, (Iwasaki et al. Paragraph 0005 Lines 10-15).

2. Referring to claim 2, a semiconductor device, wherein a film thickness of the insulating film, (Figure 4H organic low-k dielectric middle layer), on the first interlayer insulating layer, (Figure 4H inorganic low-k dielectric lower layer), is greater than that on the conductive layer, (Figure 4H the are where it is labeled metal).

3. Referring to claim 3, a semiconductor device, wherein the insulating film is made of a coating type material, (Paragraph 0100).

4. Referring to claim 5, a semiconductor device, wherein at least any one of the first interlayer insulating layer, (Figure 4H organic low-k dielectric lower layer), and the second interlayer insulating layer, (Figure 4H organic low-k dielectric upper layer), is made of an insulating material having a relative dielectric constant lower than that of an SiO_2 film, (Paragraphs 0093-0094).

5. Referring to claim 6, a semiconductor device, wherein the insulating film, (Figure 4H inorganic low-k dielectric middle layer), is made of an insulating material having a relative dielectric constant lower than that of an SiO_2 film, (Paragraph 0092).

6. Referring to claim 7, a semiconductor device, wherein the conductive layer includes a barrier metal layer, (Paragraph 0104 Lines 52-59).

7. Referring to claim 8, a semiconductor device, wherein the conductive layer includes a Cu wiring layer, (Paragraph 0104 Lines 61-63).

8. Referring to claim 10, a semiconductor device, wherein the insulating 1aym: film is made of any one of polyarylene and berlzo cyclo-butene, (Paragraph 0092 Line 17).

9. Referring to claim 31, a semiconductor device, wherein the insulating film, (Figure 4H inorganic low-k dielectric middle layer & claim 10 and Paragraph 0092 Line 17 where the film is the same material resulting in the same material properties), suppresses a progress of etching of a contact hole formed in the second interlayer insulating layer, (Figure 4H inorganic low-k dielectric upper layer), so as not to reach the first insulating layer, (Figure 4H organic low-k dielectric lower layer). AND See *** on the next page

*** Initially, and with respect to claim 31, note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); In re Fitzgerald, 205 USPQ 594, 596 (CCPA); In re Marosi et al., 218 USPQ 289 (CAFC); and most recently, In re Thorpe et al., 227 USPQ 964 (CAFC, 1985) all of which make it clear that it is the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that, as here, an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that Applicant has burden of proof in such cases as the above case law makes clear.

As to the grounds of rejection under section 103, see MPEP § 2113

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent Application Publication No. 2003/0205815 Chung. in view of U.S. Patent Application Publication No. 2004/0238965 Iwasaki et al. in further view of U.S. Patent No. 6,333,232 Kunikiyo

10. Referring to claim 9, a semiconductor device, wherein at least any one of the first interlayer insulating layer, (Figure 4H organic low-k dielectric lower layer), and the second interlayer insulating layer, (Figure 4H organic low-k dielectric upper layer), is made of methylpolysiloxane, (Chung Paragraph 0094 where it is taught a similar dielectric is used such as hydrogenmethylsiloxane).

Chung discloses the claimed invention except for the organic dielectric material being made out of methylpolysiloxane, but Kunikiyo does in Col. 26 Lines 6-13. It would have been obvious to one having ordinary skill in the art at the time the invention was made to form the low dielectric organic layer out of methylpolysiloxane, which also holds the properties of being a low k dielectric, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Victor A. Mandala Jr. whose telephone number is (571) 272-1918. The examiner can normally be reached on Monday through Thursday from 8am till 6pm..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J. Flynn can be reached on (571) 272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

VAMJ
6/9/05